Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Currently amended) A circuit for reducing jitter in a high speed serial link, the circuit comprising:

a phase-locked loop (PLL), the PLL comprising a ~~VCO~~ voltage controlled oscillator (VCO);

a regulator coupled to the PLL to provide a supply voltage to the PLL; and

a regulator control circuit coupled to the PLL and to the regulator for examining at least one parameter related to performance of the VCO, including a VCO control voltage, and for controlling adjustments of the supply voltage based on the examination.

3. (Original) The circuit of claim 2 wherein the regulator control circuit further determines if the VCO control voltage is within a predetermined range of optimum operation.

4. (Original) The circuit of claim 3 wherein the regulator control circuit further examines a lock status of the PLL.

5. (Original) The circuit of claim 4 wherein when the VCO control voltage is within the predetermined range and the PLL is locked, no adjusting of the supply voltage is done.

6. (Original) The circuit of claim 5 wherein when the VCO control voltage is not within the predetermined range or the PLL is not locked, the supply voltage is adjusted.

7. (Original) The circuit of claim 6 wherein the regulator control circuit further controls selection of a voltage level output from the regulator.

8. (Previously presented) The circuit of claim 2 wherein the regulator control circuit comprises a band gap-based reference generator coupled to comparator logic, the comparator logic coupled to measurement logic, and decision logic coupled to the measurement logic and to the comparator logic.

9. (Canceled)

10. (Previously presented) A regulator control circuit for reducing jitter in a high speed serial link, the circuit comprising:

decision logic for examining at least one parameter related to performance of a voltage controlled oscillator (VCO) in a phase-locked loop (PLL), including a VCO control voltage, comparator logic coupled to the decision logic for comparing the VCO control voltage to

predetermined voltage levels, and controlling adjustments of a supply voltage to the VCO based on the examining.

11. (Previously presented) The regulator control circuit of claim 10 further comprising a band gap-based reference generator for establishing the predetermined voltage levels.

12. (Previously presented) The regulator control circuit of claim 10 further comprising measurement logic coupled to the comparator logic for measuring an output of the comparator logic against a predetermined range of optimum operation and providing an indicator signal to the decision logic.

13. (Previously presented) The regulator control circuit of claim 12 wherein the decision logic further examines a lock status of the PLL.

14. (Previously presented) The regulator control circuit of claim 13 wherein when the decision logic determines that the VCO control voltage is within the predetermined range based on the indicator signal and that the PLL is locked based on the lock status, no adjusting of the supply voltage is done.

15. (Previously presented) The regulator control circuit of claim 14 wherein when the decision logic determines that VCO control voltage is not within the predetermined range or the PLL is not locked, the supply voltage is adjusted.

16. (Previously presented) The regulator control circuit of claim 10 wherein the decision logic further controls selection of a voltage level output of a regulator supplying voltage to the VCO.

17. (Canceled)

18. (Previously presented) A method for reducing jitter in a phase-locked loop (PLL) of a high speed serial link, the method comprising:

(a) examining at least one parameter related to performance of a voltage controlled oscillator (VCO) in the PLL, including a VCO control voltage; and

(b) controlling adjustment of a supply voltage to the VCO based on the examining.

19. (Original) The method of claim 18 wherein the examining step (a) further comprises determining if the VCO control voltage is within a predetermined range of optimum operation.

20. (Original) The method of claim 19 wherein the examining step (a) further comprises examining a lock status of the PLL.

21. (Previously presented) The method of claim 20 wherein when the VCO control voltage is within the predetermined range and the PLL is locked, no adjusting of the supply voltage is done.

22. (Previously presented) The method of claim 21 wherein when the VCO control voltage is not within the predetermined range or the PLL is not locked, the supply voltage is adjusted.

23. (Original) The method of claim 18 wherein controlling step (b) further comprises controlling selection of a voltage level output of a regulator supplying voltage to the VCO.